

Claims

- [c1] 1. A phase adjustable clock circuit comprising:
means for generating a first and a second clock signal; and
means for adjusting the phase of said first and second clock signals.
- [c2] 2. The circuit of claim 1, wherein the unadjusted phases of said first and second clock signals are 90 degrees apart.
- [c3] 3. The circuit of claim 1, wherein the phase of said first clock signal is adjusted in a phase range of ± 90 degrees and the phase of the second clock signal is not adjusted.
- [c4] 4. The circuit of claim 3, wherein the center of the phase range of said adjusted first clock signal is offset ± 90 degrees from the phase of said second clock signal.
- [c5] 5. The circuit of claim 3, wherein the amount of phase adjustment of said first clock signal is a function of magnitude of a control voltage applied to said phase adjustment circuit.
- [c6] 6. The circuit of claim 1, wherein the phase of said first clock signal is adjusted in a phase range of ± 90 degrees and the phase of the second clock signal is adjusted in a phase range of ± 90 degrees.
- [c7] 7. The circuit of claim 6, wherein the center of the phase range of said adjusted first clock signal is offset ± 90 degrees from the center of the phase range of said adjusted second clock signal.
- [c8] 8. The circuit of claim 6, wherein the amounts of phase adjustment of

said first and second clock signals are the same and are a function of the magnitude and polarity of a control voltage applied to said phase adjustment circuit.

- [c9] 9. A phase adjustable clock circuit comprising:
means for generating a first clock signal and a second clock signal; and
means for receiving said first clock signal and for generating a third clock signal from said first clock signal and means for receiving said second clock signal and for generating a fourth clock signal, wherein at least one of said third and said fourth clock signals differ in phase from said first and said second clock signal respectively.
- [c10] 10. The circuit of claim 9, wherein the phases of said first and second clock signals are 90 degrees apart.
- [c11] 11. The circuit of claim 9, wherein the phase of said third clock signal differs in a phase range of ± 90 degrees from the phase of said first clock signal and the phases of the second clock signal and fourth clock signals are the same.
- [c12] 12. The circuit of claim 11, wherein the center of the phase range of said third clock signal is offset ± 90 degrees from the phase of said fourth clock signal.
- [c13] 13. The circuit of claim 11, wherein the phase difference between said first clock signal and said third clock signal is a function of magnitude of a control voltage applied to said phase adjustment circuit.
- [c14] 14. The circuit of claim 9, wherein the phase of said third clock signal

differs in a phase range of ± 90 degrees from the phase of said first clock signal and the phase of said fourth clock signal differs in a phase range of ± 90 degrees from the phase of said second clock signal.

[c15] 15. The circuit of claim 14, wherein the center of the phase range of said third clock signal is offset ± 90 degrees from the center of the phase range of said fourth clock signal.

[c16] 16. The circuit of claim 14, wherein an amount of phase difference between said first and third clock signals is the same as an amount of phase difference between said second and fourth clock signals and is a function of the magnitude and polarity of a control voltage applied to said phase adjustment circuit.

[c17] 17. A clock and data recovery circuit comprising:
means for generating a first and a second clock signal;
means for receiving said first clock signal and for generating a third clock signal from said first clock signal and means for receiving said second clock signal and for generating a fourth clock signal, wherein at least one of said third and said fourth clock signals differ in phase from said first and said second clock signal respectively;
means for receiving said third and fourth clock signals and a serial data stream and for generating a reconstructed serial data stream and a phase error signal;
means for receiving said phase error signal and for generating a phase adjustment signal and means for receiving said phase adjustment signal by said clock generation circuit in a feedback loop to adjust the phases of

said first and second clock signals.

- [c18] 18. The circuit of claim 17, further including means for receiving said third clock signal and said reconstructed serial data stream and generating a parallel data stream.
- [c19] 19. The circuit of claim 17, wherein the phase of said third clock signal is adjustable in a phase range centered on the high/low transition of said serial data stream.
- [c20] 20. The circuit of claim 19, wherein the amount of phase adjustment of said third clock signal is a function of the magnitude and polarity of a control voltage applied to said phase adjustment circuit.
- [c21] 21. The circuit of claim 17, wherein the phase of said third clock signal is aligned to the zero transition of said serial data stream.
- [c22] 22. The circuit of claim 17, wherein the phase of said fourth clock signal is adjustable in a phase range centered on the zero transition of said serial data stream.
- [c23] 23. The circuit of claim 19, wherein the amount of phase adjustment of said fourth clock signal is a function of the magnitude and polarity of a control voltage applied to said phase adjustment circuit.
- [c24] 24. The circuit of claim 17, wherein the phases of said first and second clock signals are 90 degrees apart.
- [c25] 25. The circuit of claim 17, wherein the phase of said third clock signal differs in a phase range of +/- 90 degrees from the phase of said first

clock signal and the phases of the second clock signal and fourth clock signals are the same.

[c26] 26. The circuit of claim 25, wherein the center of the phase range of said third clock signal is offset ± 90 degrees from the phase of said fourth clock signal.

[c27] 27. The circuit of claim 25, wherein the phase difference between said first clock signal and said third clock signal is a function of the magnitude and polarity of a control voltage applied to said phase adjustment circuit.

[c28] 28. The circuit of claim 17, wherein the phase of said third clock signal differs in a phase range of ± 90 degrees from the phase of said first clock signal and the phase of said fourth clock signal differs in a phase range of ± 90 degrees from the phase of said second clock signal.

[c29] 29. The circuit of claim 28, wherein the center of the phase range of said third clock signal is offset ± 90 degrees from the center of the phase range of said fourth clock signal.

[c30] 30. The circuit of claim 28, wherein an amount of phase difference between said first and third clock signals is the same as an amount of phase difference between said second and fourth clock signals and is a function of the magnitude and polarity of a control voltage applied to said phase adjustment circuit.